IN THE CLAIMS

Please amend the claims as indicated below.

1-19. (canceled)

20. (currently amended) A method for making wafer-level chip scale package, comprising:

providing a chip pad over a substrate;

providing a re-distributed line (RDL) pattern on the chip pad;

providing an insulating layer covering a portion of the RDL pattern, wherein the insulating layer comprises a non-polymeric dielectric material; and

providing a stud bump directly on the portion of the RDL pattern not covered by the insulating layer.

21. (original) The method of claim 20, further comprising providing a solder ball on the stud bump.

22. (original) The method of claim 20, wherein the insulating layer comprises silicon nitride, silicon oxide, or silicon oxynitride.

23. (currently amended) The method of claim 20, wherein there is no under bump metal ~~between the chip pad and the RDL pattern~~.

24. (currently amended) A method for making wafer-level chip scale package, comprising:

providing a substrate with a passivation layer on a portion thereof;

forming a chip pad on a portion of the substrate not containing the passivation layer;

forming a metal layer on the chip pad and a portion of the passivation layer;

forming an insulating layer on a portion of the ~~RDL pattern~~ metal layer, wherein the insulating layer comprises a non-polymeric dielectric material; and

forming a stud bump directly on the portion of the ~~RDL pattern~~ metal layer not covered by the insulating layer.

25. (original) The method of claim 24, further comprising providing a solder ball on the stud bump.

26. (original) The method of claim 24, wherein the insulating layer comprises silicon nitride, silicon oxide, or silicon oxynitride.

27. (original) The method of claim 24, including forming the insulating layer without using a high temperature curing process.

28. (currently amended) The method of claim 24, wherein there is no under bump metal ~~between the chip pad and the RDL pattern~~.

29. (original) The method of claim 24, including forming the stud bump by an electroplating process or by wire bonding.

30. (original) The method of claim 29, including forming the stud bump by wire bonding a Pd coated copper wire to the RDL pattern using a capillary.

31. (original) The method of claim 30, wherein the wire bonding process provides the stud bump with a coined shape.

32. (currently amended) A method for making a package semiconductor device, comprising:

providing a chip pad over a substrate;

providing a re-distributed line (RDL) pattern on the chip pad;

providing an insulating layer covering a portion of the RDL pattern, wherein the insulating layer comprises a non-polymeric dielectric material; and

providing a stud bump directly on the portion of the RDL pattern not covered by the insulating layer.

33. (currently amended) A method for making an electronic apparatus containing a packaged semiconductor device, the method comprising:

providing a packaged semiconductor device containing a chip pad over a substrate, a re-distributed line (RDL) pattern on the chip pad, an insulating layer covering a portion of the RDL pattern with the insulating layer comprising a non-polymeric dielectric material, and then providing a stud bump directly on the portion of the RDL pattern not covered by the insulating layer; and

mounting the packaged semiconductor device on a circuit board.

34. (new) A method for making wafer-level chip scale package, comprising:

providing a chip pad over a substrate;

providing a re-distributed line (RDL) pattern on the chip pad;

providing an insulating layer covering a portion of the RDL pattern; and

providing a stud bump on the portion of the RDL pattern not covered by the insulating layer without using an under bump metal.

35. (new) The method of claim 34, further comprising providing a solder ball on the stud bump.

36. (new) The method of claim 34, including forming the stud bump by an electroplating process or by wire bonding.

37. (new) The method of claim 36, including forming the stud bump by wire bonding a Pd coated copper wire to the RDL pattern using a capillary.

38. (new) The method of claim 34, wherein the insulating layer comprises a non-polymeric dielectric material.

39. (new) The method of claim 38, wherein the insulating layer comprises silicon nitride, silicon oxide, or silicon oxynitride.

40. (new) The method of claim 34, including forming the insulating layer without using a high temperature curing process.

41. (new) A method for making wafer-level chip scale package, comprising:

providing a chip pad over a substrate;

providing a single-layer re-distributed line (RDL) pattern on the chip pad;

providing an insulating layer covering a portion of the RDL pattern; and

providing a stud bump on the portion of the RDL pattern not covered by the insulating layer.

42. (new) The method of claim 41, further comprising providing a solder ball on the stud bump.

43. (new) The method of claim 41, including forming the stud bump by an electroplating process or by wire bonding.

44. (new) The method of claim 43, including forming the stud bump by wire bonding a Pd coated copper wire to the RDL pattern using a capillary.

45. (new) The method of claim 41, wherein the insulating layer comprises a non-polymeric dielectric material.

46. (new) The method of claim 45, wherein the insulating layer comprises silicon nitride, silicon oxide, or silicon oxynitride.

47. (new) The method of claim 41, including forming the insulating layer without using a high temperature curing process.